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# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

Total Number of Pages in This Submission

| | |
|---|---|
| Application Number | 10/086,980 |
| Filing Date | March 1,2002 |
| First Named Inventor | Osman Kent |
| Art Unit | 2671 |
| Examiner Name | Tung, Kee M. |
| Attorney Docket Number | TD-168 |

## ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
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  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☑ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

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Remarks

Response to Notification of Non-Compliance With Requirement of 37 CFR 41.37(c) (Re-submission of Appeal Brief with Appendices A to E)

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | | | |
|---|---|---|---|
| Firm Name | Groover & Holmes | | |
| Signature | | | |
| Printed name | Patrick C.R. Holmes | | |
| Date | November 17, 2005 | Reg. No. | 46,380 |

## CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

| | | | |
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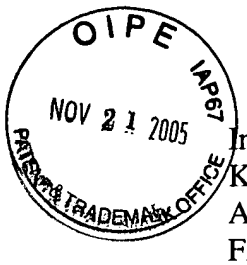
| Signature | | | |
| Typed or printed name | Patrick C.R. Holmes | Date | November 17, 2005 |




In the United States Patent and Trademark Office

In re application of: :
Kent, Osman : Art Unit: 2676
AN 10/086,980 : Examiner: Tung, Kee M.
Filed: 03/01/2002 : Atty's Docket: TD-168

For: Yield Enhancement of Complex Chips (As Amended)

APPEAL BRIEF

Honorable Commissioner of Patents and Trademarks
Alexandria, VA 22313

Sir:

In response to the Notification of Non-Compliance With The Requirement of 37 CFR 41.37(c) dated October 20, 2005, enclosed is an Appeal Brief with five Appendices (including a copy of the Notice of Appeal previously filed). Docketing for Oral Argument is requested.

Any extension of time necessary for consideration of this appeal is also hereby requested. The correct amount of fee has been paid previously. However, the Commissioner is authorized to charge any fees, or credit any overpayment, to Deposit Account Number 07-2320.

## Table of Contents

## Table of Authorities

### Cases



### Statutes



### United States Patents

**Real Party in Interest**

The real party in interest, and assignee of this case, is *3Dlabs Inc., Ltd.*, of Reid Hall, Hamilton HM11, Bermuda.

**Related Appeals and Interferences**

To the best knowledge and belief of the undersigned attorney, there are no related appeals or interferences.

**Status of Claims**

Claims 1,3-5 and 7-35 are pending and are each under final rejection. No other claims are pending. Each claim is appealed.

**Status of Amendments after Final**

An amendment after final rejection was submitted on October 8, 2004. The amendment was not entered, as stated in correspondence from the Office dated 11/9/2004.

**Summary of Invention**

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

The claimed subject matter of independent claim 1 can be summarized as a graphics processor (described repeatedly throughout the specification, *e.g.*, p. 3, line 9 *et al.*) with more than one graphics computational units, such as vertex processors, texture pipes, memory controllers, and RAMDACs (*see*, for example, p. 6 line 27-p. 7 line 1; *see* also Figure 1). (It is noted that these units are shown in Figure 1, but are described using text and not reference numbers; therefore, reference numbers are not provided.) Further, claim 1 recites a task allocation unit programmed to bypass defective units of the graphics processor (p. 6, lines 19-22; p. 44, lines 15-18) that provides reconfigurability in the architecture, so that incoming tasks can be distributed only among operative units and not defective units (p.44 lines 15-18).

Independent claim 12 recites a method of graphics rendering comprising multiple parallelized graphics computational units such as vertex processors, texture pipes, memory controllers, and RAMDACs (*see*, for example, p. 6 line 27-p. 7 line 1; *see* also Figure 1). Some of these units, if defective, are bypassed (p. 7 lines 3-6), and incoming tasks are distributed among operative units (p. 7, lines 3-6).

Independent claim 20 includes "means for" providing multiple parallelized graphics computational units such as vertex processors, texture pipes, memory controllers, and RAMDACs (*see*, for example, p. 6 line 27-p. 7 line 1; *see* also Figure 1); means for bypassing defective units (for example, if manufacturing creates defects)

of the graphics processor (p. 6, lines 19-22; p. 44, lines 15-18) so that incoming tasks can be distributed only among operative units and not defective units (p.44 lines 15-18).

Independent claim 28 recites a method for a computer graphics system operation with the steps of providing a plurality of parallelized rendering units such as vertex processors, texture pipes, memory controllers, and RAMDACs (*see*, for example, p. 6 line 27-p. 7 line 1; *see* also Figure 1). Some of these units, if defective, are bypassed (p. 7 lines 3-6), and incoming tasks are distributed among operative units (p. 7, lines 3-6).

**Grounds of Rejection to be Reviewed on Appeal**

Are claims 1, 3-5 and 7-35 that have been rejected under 35 U.S.C. §103(a) as unpatentable over Baldwin (6,025,853) in view of Brent et al (5,459,864)?

**Review of the References**

Baldwin (U.S. Patent No. 6,025,853) relates to a processing chip that uses a deep pipeline of multiple asynchronous units to achieve a high net throughput in 3D rendering.

Brent et al. (U.S. Patent No. 5,459,864) relates to load balancing, recovery and reconfiguration control for a data move subsystem.

If the undersigned attorney has overlooked a relevant teaching in any of the references, the Examiner is requested to point out very specifically where such teaching may be found.

## ARGUMENT

**Issue: Are claims 1, 3-5 and 7-35 unpatentable over Baldwin (6,025,853) in view of Brent et al (5,459,864) under 35 U.S.C. 103(a)?**

***Requirements for Rejection under 35 USC 103(a)***

A fundamental notion of patent law is the concept that invention lies in the new combination of old elements. Therefore, a rule that every invention could be rejected as obvious by merely locating each element of the invention in the prior art and combining the references to formulate an obviousness rejection is inconsistent with the very nature of "invention." Consequently, a rule exists that a combination of references made to establish a *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention.

The inquiry is not whether each element existed in the prior art, but whether the invention as a whole is obvious in light of the prior art. *Hartness International, Inc. v. Simplimatic Engineering Co.*, 819 F.2d 100, 2 U.S.P.Q.2d 1826 (Fed. Cir. 1987). The examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992).

***Overview of the Rejection under 35 USC 103(a)***

Claims in groups A, B, C, and D all stand rejected under 35 USC Section 103(a) as being unpatentable over *Baldwin* in view of *Brent et al.* For the purpose of clarity, the independent claim of each group is reproduced below.

Claim 1, representative of Group "A" are dependant, is reproduced below.

A graphics processor, comprising:

a plurality of parallelled graphics computational units; and

one or more task allocation units programmed to bypass defective ones of said units within said groups, and to distribute incoming tasks only among operative ones of said units.

Claim 12, representative of Groups "B", "C", and "D" is reproduced below.

A method of 3D graphics rendering, comprising the actions of:

providing a plurality of parallellized graphics computational units;

bypassing defective ones of said units, and

distributing incoming tasks only among operative ones of said units.

## I. The combination of the cited references do not teach or suggest all limitations of the claims of Groups A, B, C or D.

The combination of the Baldwin and Brent references do not teach or suggest all limitations of, for example, claim 1. Claim 1 claims in part "a plurality of paralleled graphics computational units" which is part of a single processor. Brent's teaching deals with the allocation between separate processors, while Baldwin deals with the allocation within a single processor. As argued below, the combination of the Brent and Baldwin references does not teach or suggest a singe processor with the limitations of claim 1.

As determined in *Thrift,* [1] a rejection which "does not discuss the unique limitations" of the claims was held to be "simply inadequate on its face." In this case, a rejection was held "not supported by substantial evidence because the cited references do not support each limitation of claim 11." See *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1443 (Fed. Cir. 1991)."[2] In the present case, the examiner has failed to address the unique limitations of *a graphics processor ... with one or more task allocation units programmed to bypass defective ones of said units.* Therefore, a prima facie case of obviousness has not been established by the Examiner.

Claim Groups A, B, C, and D all are directed towards a processor with "A single processor, with parallel functions" that was previous pictured in the original application as follows:

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[1] *In re Thrift*, 298 F.3d 1357 (Fed.Cir. 2002).

[2] *In re Thrift,* 298 F.3d at 1366 (emphasis added).

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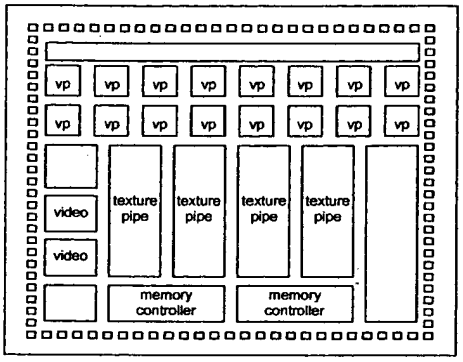



FIG. 1

As illustrated, this single processor is a die component that is comprised of several texture pipes controlled by an internal task allocation unit.

The way that this processor controls data was shown in figure 1B. This figure illustrates the "*a plurality of parallellized graphics computational units*" as shown by Texture Pipe 0 through Texture Pipe N. The "*task allocation units*" are shown in the "Router" function which enables the processor to bypass defective Texture Pipes. It is the Router unit that, in this embodiment, allows the processor to bypass a defective pipeline within the processor.

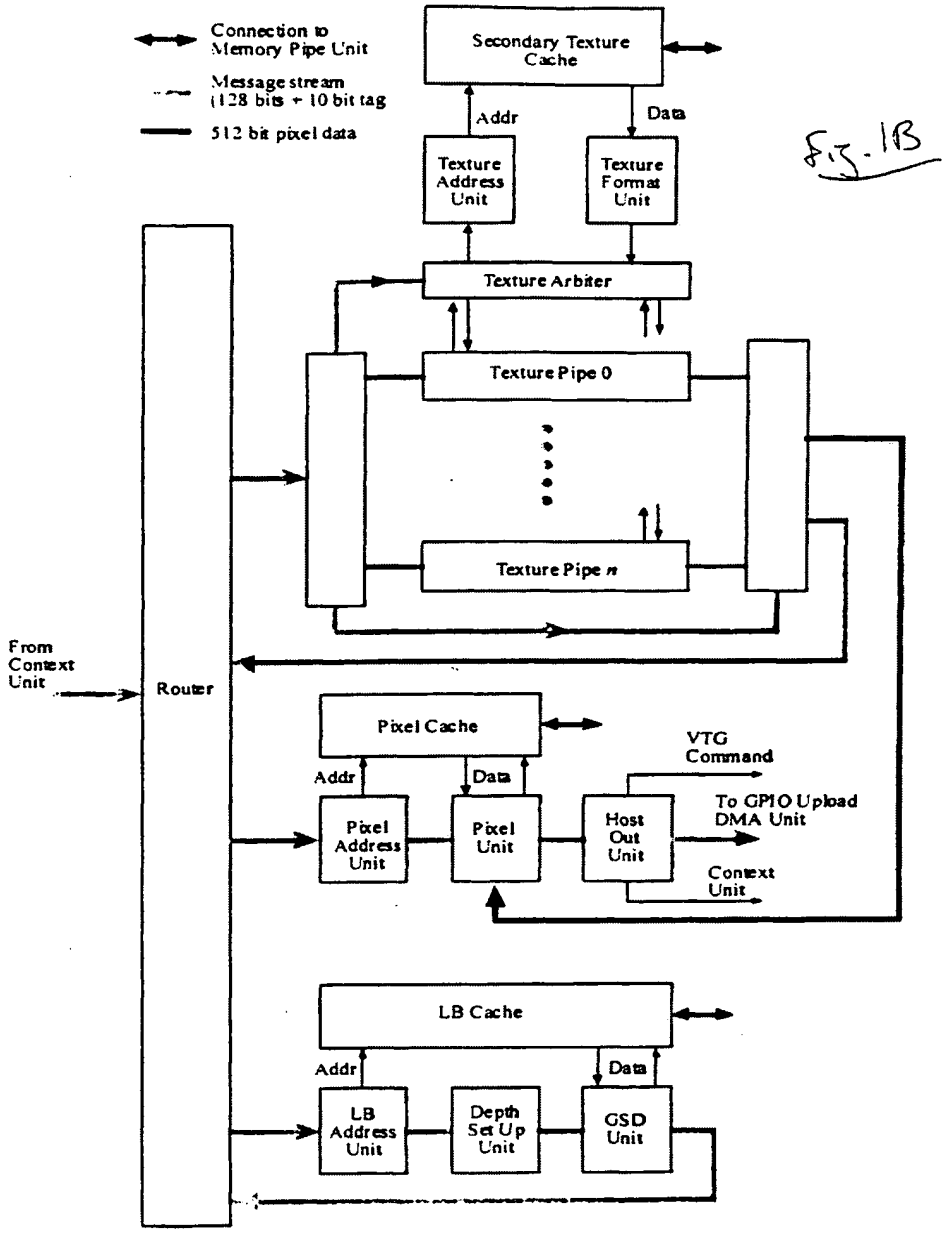
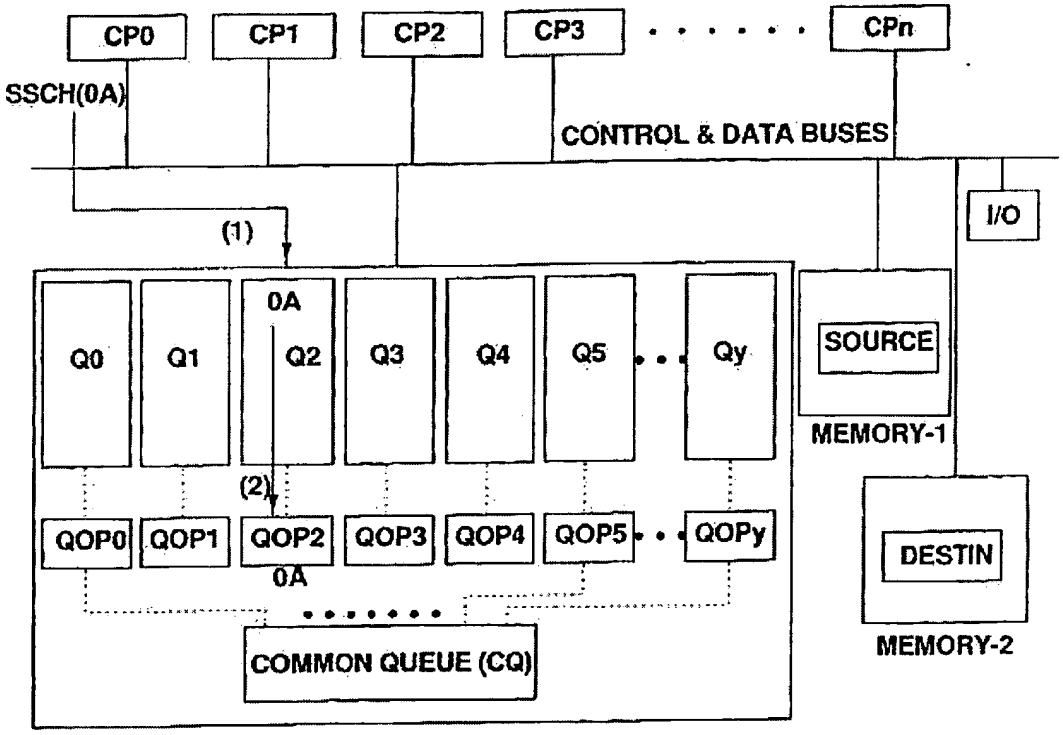



Fig. 1B

In contrast, the prior art teaches away from the present inventions as it not only operates on a completely different scale, but also requires a plurality of processors in order to function. The Brent patent requires a multiple of separate, fully functional processors in order to function. This is the "***PLURAL QUEUE***

***PROCESSORS"*** requirement that is named in Brent application. Figure 2 of the Brent patent illustrates this, and is reproduced below:

FIG.2




The entire present application would be placed within any one of the CP0, CP1, etc. elements within the Figure 2 of the Brent Application. In the prior art if a cpu were to fail, it would be eliminated completely from the system. The Brent solution to a failed pipeline is to disable the entire processor, whereas in the present invention the solution is to disable only the pipeline leaving the remainder of the processor to function. The Brent solution is like amputating a limb in the case of a broken artery in order to save the body, wherein the present application can close the artery and save the limb.

If the prior art cited references were combined, they would only create an extension of the Brent reference. This would not allow for the disabling of a partially defective processor, and would require the removal of an entire processor unit.

Moreover, in the '864 patent the processor failure must occur while the processor is running, wherein the current invention a diagnostic can be preformed to detect the error, and the failure can be prevented prior to the processor even leaving the factory. This feature was also noted in the original application.

> "To allow this to be implemented we need to have reconfigurability in the architecture, independent scan chains so that a manufacturing fault can be isolated and a method of recording the test result inside the chip."[3]

This is another good example of the differences between the present inventions which can prevent failure even when there is a faulty component, and the prior art which teaches simply to disable the entire component.

The only way that the examiner can reach the present invention is by making significant modifications to the cited references. The mere fact that a prior art reference can be readily modified does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 U.S.P.Q.2d 1397 (Fed. Cir. 1989) and also see In re Fritch, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992) and In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1993). The examiner may not merely state that the modification would have been obvious to one of ordinary skill in the art without pointing out in the prior art a suggestion of the desirability of the proposed modification.

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[3] Page 3, Lines 23-25, of the Original Application, Atty Docket TD-168

In the present case, Examiner has neither suggested the necessary modifications, nor has pointed to any suggestion in the references to make such modifications.

Therefore, the combination of the Baldwin and Brent references do not teach or suggest all limitations of, for example, claim 1. As previously stated, claim 1 claims in part "a plurality of paralleled graphics computational units" which is part of a single processor. Brent's teaching deals with the allocation between separate processors, while Baldwin deals with the allocation between units of a single processor. Even if properly combined, these references together do not teach all of the limitations of claim 1. Hence, the combination of the Brent and Baldwin references do not teach or suggest a singe processor with the limitations of claim 1, or the other inventions disclosed by the applicant. This argument applies equally to all claim groups, including Groups A, B, C, and D.

## II. There Is No Teaching or Suggestion In The Cited References To Combine The Cited References

There is no teaching or suggestion to combine the cited references to form the inventions found in Group A, B, C or D. In determining obviousness, an applicant's teachings may not be read into the prior art. Panduit Corp. v. Denison Mfg. Co., 810 F.2d 1561, 1575 n. 29, 1 U.S.P.Q. 1593, 1602 n. 29 (Fed. Cir. 1987) (citing need to "guard against hindsight and the temptation to read the inventor's teachings into the prior art"). A determination of the desirability of combining prior art references must be made without the benefit of hindsight afforded by an applicant's disclosure. In re Paulsen, 30 F.3d 1475, 1482, 31 U.S.P.Q. 1671, 1676 (Fed. Cir. 1994).

Applicants aver that examiner could not have reached the proposed combination without using the present invention as a template. This is an impermissible use of hindsight.

Examiner Tung writes in his rejection that:

> *"Brent teaches a load balancing, error recovery and reconfiguration control in a data movement subsystem with cooperating plural queue processors (Fig. 2, abstract, col. 2, lines 39-45, col. 5, lines 49-52 and col. 6, lines 11-18). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of bypass defective unit and distribute load from defective unit to other units of Brent into the system of Baldwin in order to automatic load balancing among plural processors, automatic recovery from any failing processor, and automatic reconfiguration for the subsystem containing the processors without intervention from the operating system as taught by Brent (col. 1, lines 18-24). Therefore, at least claims 1, 3-5 and 7 would have been obvious[4]."*

This assertion that it is obvious to combine the prior art is flawed for at least two reasons. First, the '864 requires "plural queue processors"[5] in order to recover from any "failing queue processor"[6]. The '864 is designed to recover from a fatal error in a multi-processor environment. The present invention is designed to actively disable a section of an otherwise defective processor in order to make it functional. This was highlighted in the following passage from the original application:

> "During testing a single bit error anywhere on the die will force that die to be scrapped... However, by internally reconfiguring the chip we can still make use of a die with one or more failing texture pipes, for example. This allows us to take die which would otherwise be classified as scrap and use them in a lower performance product."[7]

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[4] Id.

[5] US Patent 5,459,864, Col 1, line 18-20.

[6] Id.

[7] Page 3, Lines 15-22, of the Original Application, Atty Docket TD-168.

The '864, when encountering an error within a queue processor, reconfigures to avoid the failed processor – including shutting down possibly operable pipelines. The patent states this point in the following passage:

> *"...the failing processor is stopped, removed from the operational sub- 50 system, and its work redistributed to other processors through the subsystem workload balancing process."*[8]

The relevant cited prior art only applies when a total processor failure occurs, whereas the present application prevents the processor failure by preemptively removing defective pipelines thereby allowing the processor to function. In the event of a processor failure, the '864 patent requires that "the failing processor is stopped, removed from the operational subsystem"[9], whereas in the present inventions allow for "use partially defective die as fully functioning parts with lower performance"[10]

Thus, the teachings of the Baldwin and Brent references are clearly incompatible, because they apply to difference scales – Baldwin deals with incompatible units at a single processor, while Brent deals with separate, individual processors and does not address computational unit is within those processors.

The second reason that it is not obvious to combine the cited reference is that there is no statement, method, or suggestion in those references for such a combination. No such statement, motive, or suggestion is found in the references.

A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the

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[8] US Patent 5,459,864, Col 5, line 47-52.

[9] US Patent 5,459,864, Col 5, line 48-52.

[10] Page 4, Lines 3-5, of the Original Application, Atty Docket TD-168.

combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990).

Therefore, the cited references are not properly combinable because there is no statement, motive, or suggestion to make the combination.

## III. The Cited References Cannot be Properly Combined as the Examiner suggests.

As argued above, Brent deals with the allocation of tasks between multiple processors, while Baldwin deals with the allocation of tasks within a single processor. The difference in the magnitude of scale is made more clear below.

### A. The cited references cannot be combined to form the inventions found in Group A.

The asserted combination of references does not support each limitation of the independent claim found in Group A. Specifically, Claim 1 recites "**a plurality of paralleled graphics computational units; and one or more task allocation units programmed to bypass defective ones of said units within said groups, and to distribute incoming tasks only among operative ones of said units.**"

Examiner Tung begins his rejection of Group A under 103(a) by pointing out that *"Baldwin fails to explicitly teach or suggest one or more task allocation units*

*programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits.*[11]"

This admission, that the Baldwin art fails to teach the distribution of tasks when a processor has a defective pipeline, highlights one of the differences between the prior art and the present inventions that teaches "*graphics processor, comprising a plurality of parallelled graphics computational units and one or more task allocation units programmed to bypass defective ones of said units.*" The Baldwin reference requires that all parallel subunits function properly whereas in the present inventions the processor will continue to function, albeit at a reduced capacity, by disabling a subunit.

Examiner Tung attempts to cure this defect by applying the *Brent et al* reference. However, *Brent et al.* does not disclose or suggest one or more task allocation units to bypass defective graphics computational units and to distribute incoming tasks only among operative graphics computational units. The Examiner has correctly noted that *Brent et al.* teaches a load balancing, error recovery and reconfiguration control in a ***data movement subsystem with cooperating plural queue processors***. Brent does not teach a process by which a single processor may continue to function even though it is partially defective. There is no suggestion to use a partially operative single processor in any of the cited prior art. Instead, Brent teaches away from this innovation because in order to function it requires a processor that is partially defective to be completely disabled, whereas in the present inventions, the partially operable processor is allowed to continue to function within a system. Using out invention as a template is an impermissible use of hindsight.

[11] Page 2 of the office action dated August 5, 2005

***A System using "plural queue processors" to compensate for the failure of a graphics processor does not teach or suggest "A graphics processor with one or more task allocation units programmed to bypass defective ones."***

There is a delineation that needs to be made between the example the Examiner Tung alludes to wherein there is a plurality of queue processors, and the present invention wherein ***A GRAPHICS PROCESSOR WITH ONE OR MORE TASK ALLOCATION UNITS PROGRAMMED TO BYPASS DEFECTIVE ONES.***

In the rejection of the claims, Examiner Tung asserts that: "*It is old and well known and well used in the art to dynamically load balanced among multiple processors include skip or bypass defective unit(s)*[12]."

This application deals with the ability to bypass a defective pipeline within a SINGLE processor ("A GRAPHICS PROCESSOR") as opposed to the MULITIPLE ("*PLURAL QUEUE PROCESSORS*") processors alluded to in the prior art.

Therefore, the examiner has failed to show that the cited references are capable of being properly combined. Moreover, even if the examiner can show that such a combination is possible, a position that the applicant strongly disagrees with, the combination of such cited references would lead to an invention directed towards a system of multiple processors rather than the single processor solution disclosed by the inventor.

[12] id.

**B. The cited references cannot be combined to form the inventions found in Groups B,C, and D.**

Examiner does not individually address the inventions in Group B, C, or D in his rejection, and instead reiterates the arguments he has made to his rejection of Group A. Just as the recited references cannot be combined to for the inventions found in Group A, the references cannot be combined to form the inventions found in Group B, C, or D.

The independent claim of Group B reads "**A method of 3D graphics rendering, comprising the actions of providing a plurality of parallellized graphics computational units; bypassing defective ones of said units, and distributing incoming tasks only among operative ones of said units.**" There is no background in the prior art to have a graphics processor with multiple graphics computational units within the single processor, where there can be the bypassing of some of the units during operation.

Claim 20, from which all claims in Group "C" depend, claims the inventions of a computer graphics system comprising means for providing a plurality of parallellized graphics computational units means for bypassing defective ones of said units, and means for distributing incoming tasks only among operative ones of said units. Again, there is no background in the prior art to have a graphics processor with multiple graphics computational units within the single processor, where there can be the bypassing of some of the units during operation.

Claim 28, from which all claims in Group "D" depend, claims a method for computer graphics system operation, comprising the actions of providing a plurality of parallellized rendering units bypassing defective ones of said units, and distributing incoming tasks only among operative ones of said units. Again, there is no background in the prior art to have a graphics processor with multiple graphics computational units within

the single processor, where there can be the bypassing of some of the units during operation.

The specification clearly states that each one of these computational units are subparts of a single processor unit. The original specification discloses this innovative feature when it states "A graphics processor, comprising: a plurality of parallellized graphics computational units"[13] Examiner Tung has applied his rejection to claim continues in his rejection to correctly points out that *"Baldwin fails to explicitly teach or suggest one or more task allocation units programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits.*[14]"

This admission, that the Baldwin art fails to teach the distribution of tasks when a processor has a defective pipeline, highlights one of the differences from the present inventions that teaches "*graphics processor, comprising a plurality of parallelled graphics computational units and one or more task allocation units programmed to bypass defective ones of said units.*" The Baldwin reference requires that all parallel subunits function properly whereas in the present inventions the processor will continue to function, albeit at a reduced capacity, by disabling a subunit.

Examiner Tung attempts to cure this defect by applying the *Brent et al* reference. However, *Brent et al.* does not disclose or suggest one or more task allocation units to bypass defective graphics computational units and to distribute incoming tasks only among operative graphics computational units. The Examiner has correctly noted that *Brent et al.* teaches a load balancing, error recovery and reconfiguration control in a ***data movement***

[13] Page 44, Lines 14-15, of the Original Application, Atty Docket TD-168.
[14] Page 2 of the office action dated August 5, 2005

***subsystem with cooperating plural queue processors***. Brent does not teach a process by which a single processor may continue to function even though it is partially defective. There is no suggestion to use a partially operative processor. Instead, Brent teaches away from this innovation and it requires a processor that is partially defective to be disabled within a system.

Therefore, the examiner has failed to show that the cited references are capable of being properly combined. Moreover, even if the examiner can show that such a combination is possible, a position that the applicant strongly disagrees with, the combination of such cited references would lead to an invention directed towards a system of multiple processors rather than the single processor solution disclosed by the inventor.

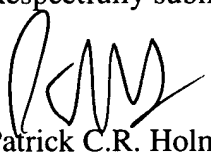
Therefore, for all of the above reasons, applicants respectfully submit that Examiner has failed to make out a *prima facie* case of obviousness.

**Requested Relief**

For the reasons advanced above, Appellant respectfully contends that claims 1, 3-5 and 7-35 are patentable. Therefore, reversal of this rejection is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection of this paper, including extension of time fees, to Deposit Account 07-2320 and please credit any excess fees to such deposit account.

Respectfully submitted,



Patrick C.R. Holmes
Registration No. 46,380
Attorney for Appellant

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Osman Kent :: Art Unit: 2676

Application No.: 10/086,980 : Examiner: Tung, Kee M.

Filed: 03/01/2002 : Atty's Docket: TD-168

For: Yield Enhancement of Complex Chips (confirmation no. 6304)

APPENDIX A – Text of Claims on Appeal

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (previously amended): A graphics processor, comprising:

a plurality of parallellized graphics computational units; and

one or more task allocation units programmed to bypass defective ones of said units within said groups, and to distribute incoming tasks only among operative ones of said units.

2. (canceled)

3. (previously amended): The graphics processor of claim 1, wherein each of_said parallellized graphics computational units also includes respective_multiple vertex processors.

4. (previously amended): The graphics processor of claim 1, wherein each of said parallellized graphics computational units also includes respective_texturing pipelines.

5. (previously amended): The graphics processor of claim 1, wherein each of said parallellized graphics computational units also includes a respective_memory controller.

6. (canceled)

7. (original): A method of 3D graphics rendering which comprises: using a task allocation unit and parallellized graphics computational units with relations as recited in claim 1.

8. (previously submitted): The graphics processor of claim 1, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative vertex processors.

9. (previously submitted): The graphics processor of claim 1, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative texturing pipelines.

10. (previously submitted): The graphics processor of claim 4, wherein said texturing pipelines also include a shading unit and a texture filter unit.

11. (previously submitted): The graphics processor of claim 4, wherein said texturing pipelines also include a shading unit and a primary texture cache.

12. (previously submitted): A method of 3D graphics rendering, comprising the actions of:

providing a plurality of parallellized graphics computational units;

bypassing defective ones of said units, and

distributing incoming tasks only among operative ones of said units.

13. (previously submitted): The method of claim 12, wherein each of said parallellized graphics computational units also includes respective multiple vertex processors.

14. (previously submitted): The method of claim 12, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative vertex processors.

15. (previously submitted): The method of claim 12, wherein each of said parallellized graphics computational units also includes respective multiple texturing pipelines.

16. (previously submitted): The method of claim 12, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative texturing pipelines.

17. (previously submitted): The method of claim 12, wherein each of said parallellized graphics computational units also includes a respective memory controller.

18. (previously submitted): The method of claim 15, wherein said texturing pipelines also include a shading unit and a texture filter unit.

19. (previously submitted): The method of claim 15, wherein said texturing pipelines also include a shading unit and a primary texture cache.

20. (previously submitted): A computer graphics system comprising:

means for providing a plurality of parallellized graphics computational units;

means for bypassing defective ones of said units, and

means for distributing incoming tasks only among operative ones of said units.

21. (previously submitted): The system of claim 20, wherein each of said parallellized graphics computational units also includes respective multiple vertex processors.

22. (previously submitted): The system of claim 20, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative vertex processors.

23. (previously submitted): The system of claim 20, wherein each of said parallellized graphics computational units also includes respective multiple texturing pipelines.

24. (previously submitted): The system of claim 20, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative texturing pipelines.

25. (previously submitted): The system of claim 20, wherein each of said parallellized graphics computational units also includes a respective memory controller.

26. (previously submitted): The system of claim 23, wherein said texturing pipelines also include a shading unit and a texture filter unit.

27. (previously submitted): The system of claim 23, wherein said texturing pipelines also include a shading unit and a primary texture cache.

28. (previously submitted): A method for computer graphics system operation, comprising the actions of:

providing a plurality of parallellized rendering units;

bypassing defective ones of said units, and

distributing incoming tasks only among operative ones of said units.

29. (previously submitted): The method of claim 28, wherein each of said parallellized rendering units also includes respective multiple vertex processors.

30. (previously submitted): The method of claim 28, wherein one or more of said parallellized rendering units operate with no more than 4 operative vertex processors.

31. (previously submitted): The method of claim 28, wherein each of said parallellized rendering units also includes respective multiple texturing pipelines.

32. (previously submitted): The method of claim 28, wherein one or more of said parallellized rendering units operate with no more than 4 operative texturing pipelines.

33. (previously submitted): The method of claim 28, wherein each of said parallellized rendering units also includes a respective memory controller.

34. (previously submitted): The method of claim 31, wherein said texturing pipelines also include a shading unit and a texture filter unit.

35. (previously submitted): The method of claim 31, wherein said texturing pipelines also include a shading unit and a primary texture cache.

APPENDIX C – Copy of Notice of Appeal previously filed

PTO/SB/21 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

Total Number of Pages in This Submission: 3

| | |
|---|---|
| Application Number | 10/086,960 |
| Filing Date | 03/01/2002 |
| First Named Inventor | Kent |
| Art Unit | 2676 |
| Examiner Name | |
| Attorney Docket Number | TD-168 |

## ENCLOSURES (Check all that apply)

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☑ Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosure(s) (please identify below):

Remarks

## SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

| | | | |
|---|---|---|---|
| Firm Name | Groover & Holmes | | |
| Signature | N. Pham | | |
| Printed name | N. Elizabeth Pham | | |
| Date | 01/04/2005 | Reg. No. | 49,042 |

## CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

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|---|---|---|---|
| Signature | Peggy Heath | | |
| Typed or printed name | Peggy Heath | Date | 01/04/2005 |

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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# NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): TD-168

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]
on January 4, 2005
Signature: Peggy Heath
Typed or printed name: PEGGY HEATH

In re Application of: Kent
Application Number: 10/086,980
Filed: 03/01/2002
For: Yield enhancement of Complex Chips
Art Unit: 2676
Examiner:

Applicant hereby appeals to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 500.00

- ☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____
- ☐ A check in the amount of the fee is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.
- ☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 07-2320. I have enclosed a duplicate copy of this sheet.
- ☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

**WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 49,042
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

N. Elizabeth Pham
Signature
N. Elizabeth Pham
Typed or printed name
972-980-5840
Telephone number
1-4-05
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☑ *Total of 2 forms are submitted.

APPENDIX D– Copy of Application Drawings

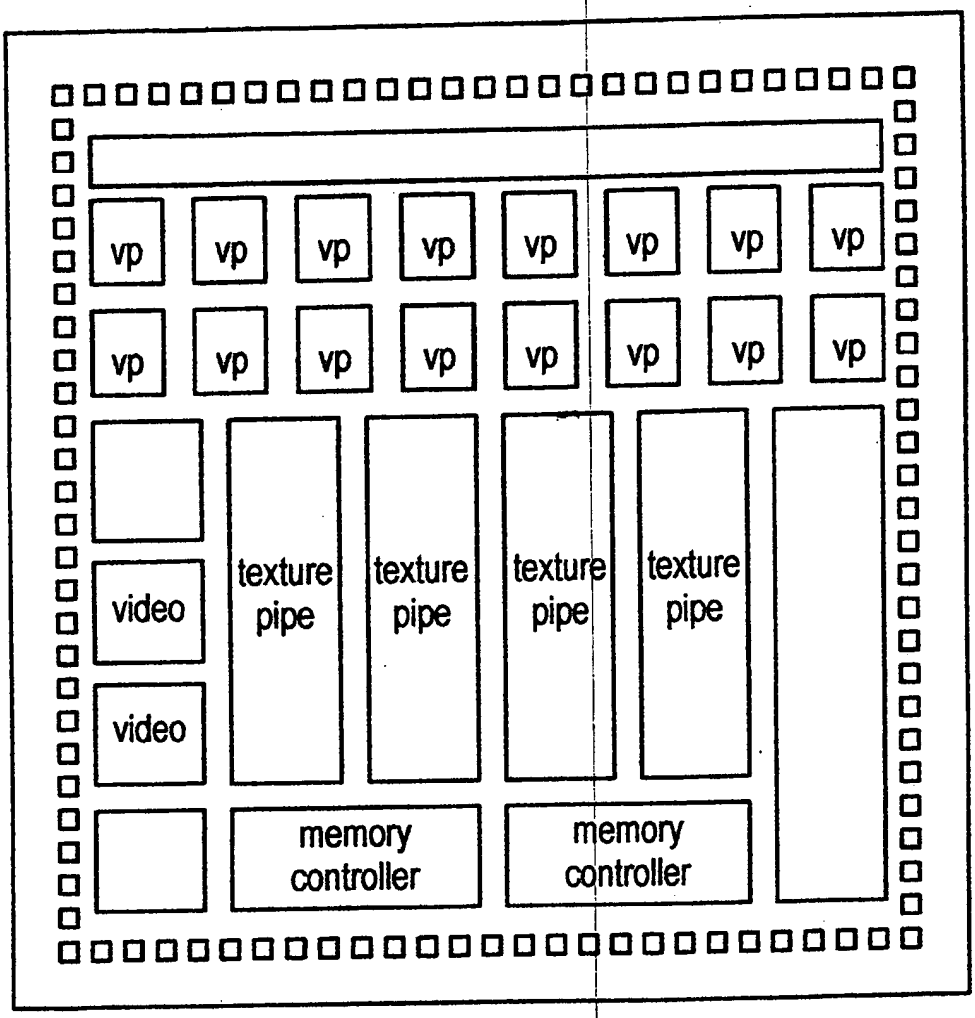


FIG. 1

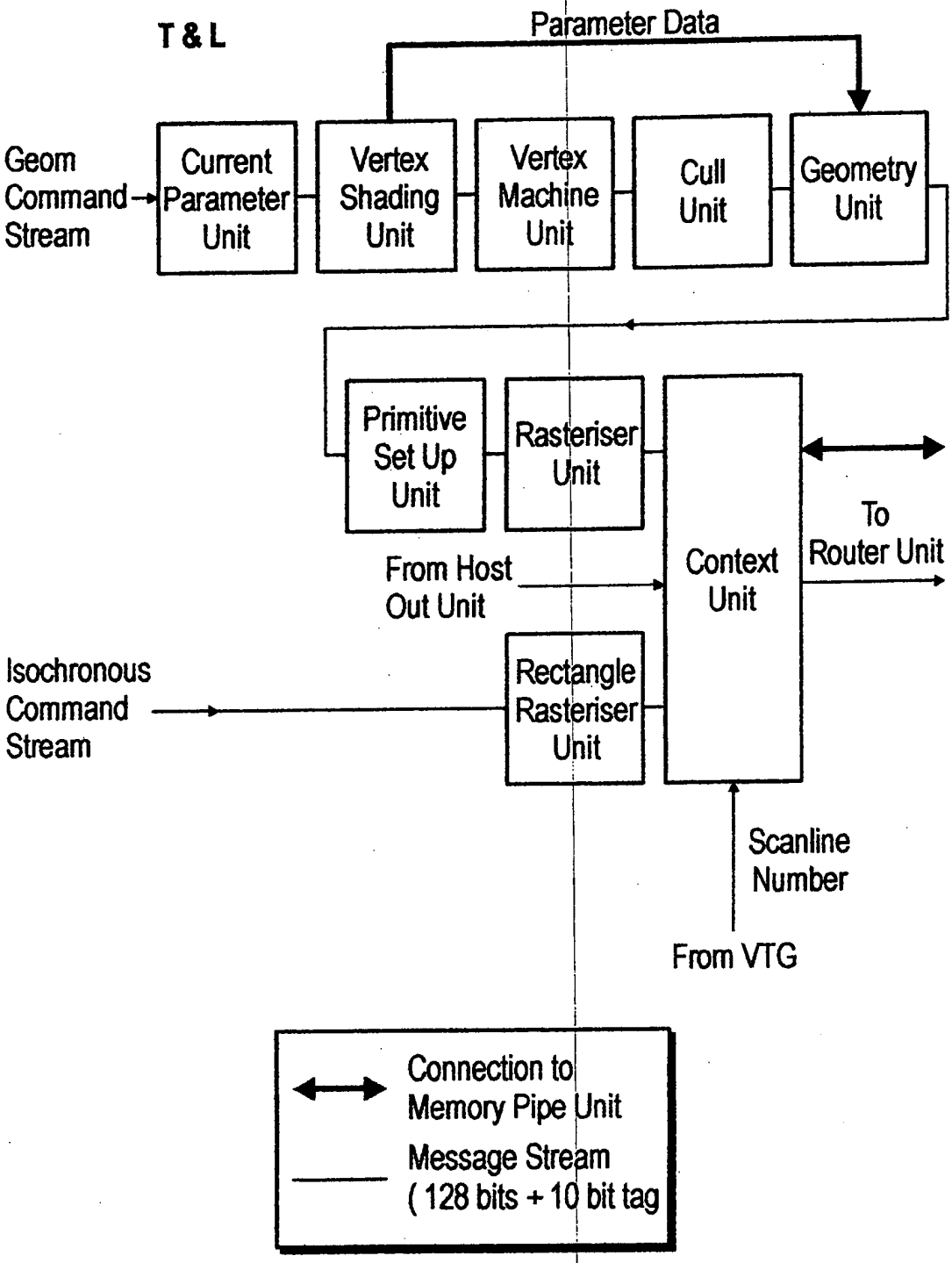


FIG. 1A

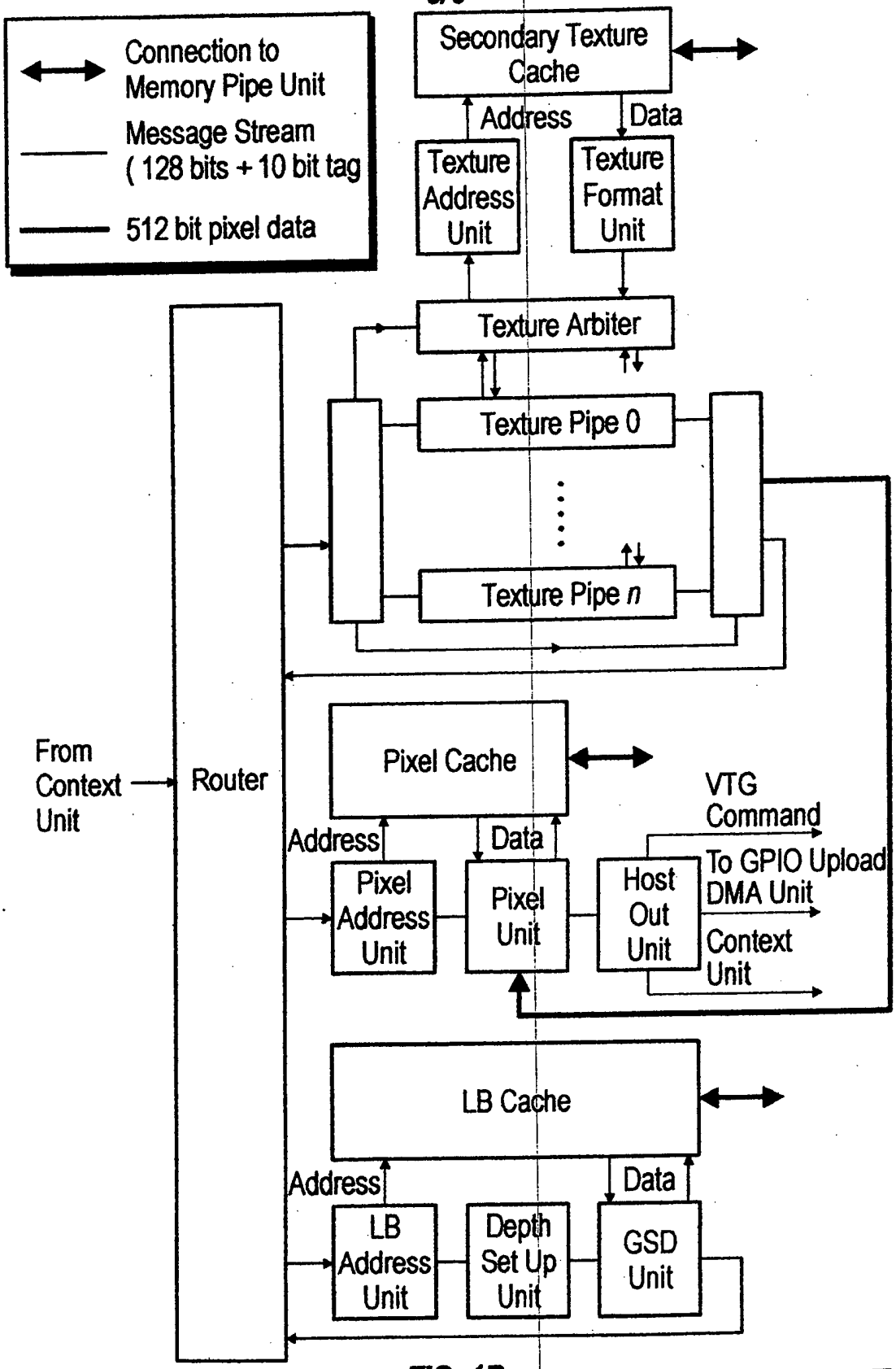


FIG. 1B

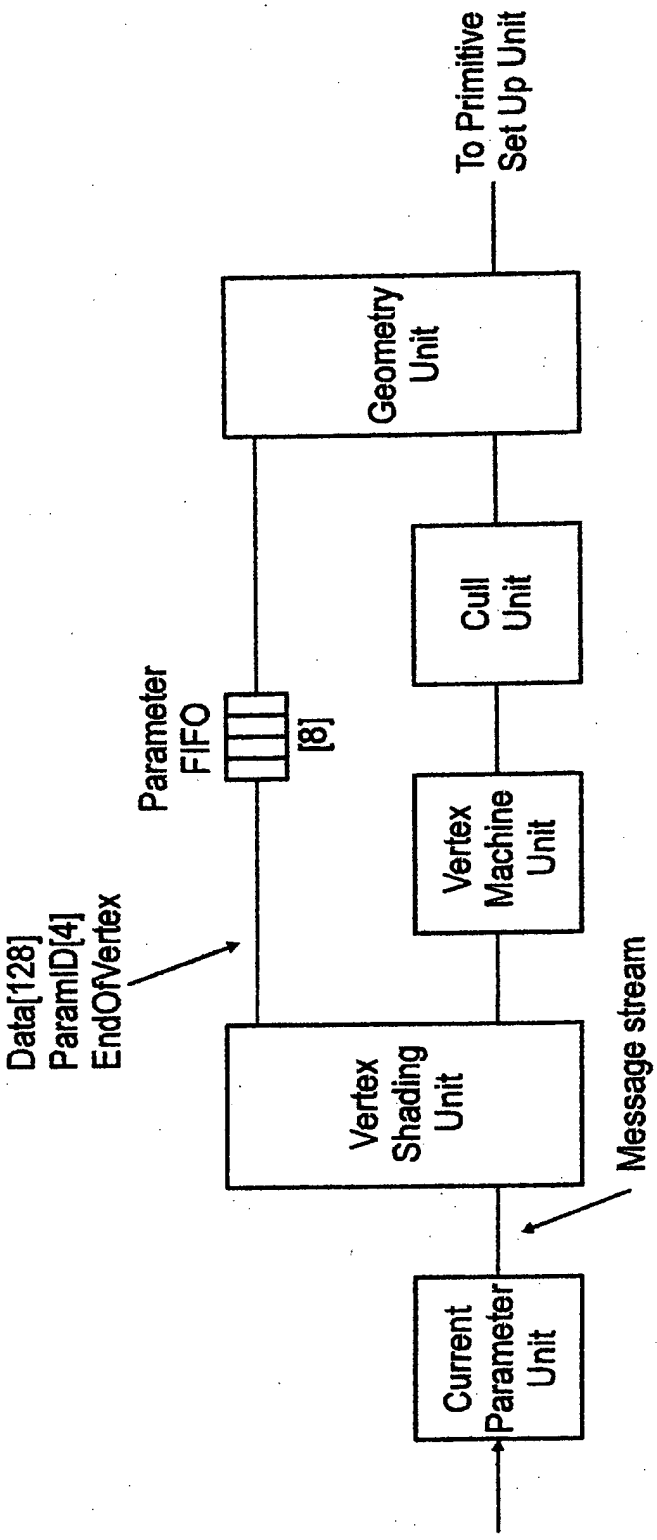
To Primitive Set Up Unit
Geometry Unit
Cull Unit
Vertex Machine Unit
Parameter FIFO [8]
Data[128] ParamID[4] EndOfVertex
Vertex Shading Unit
Message stream
Current Parameter Unit

FIG. 1C

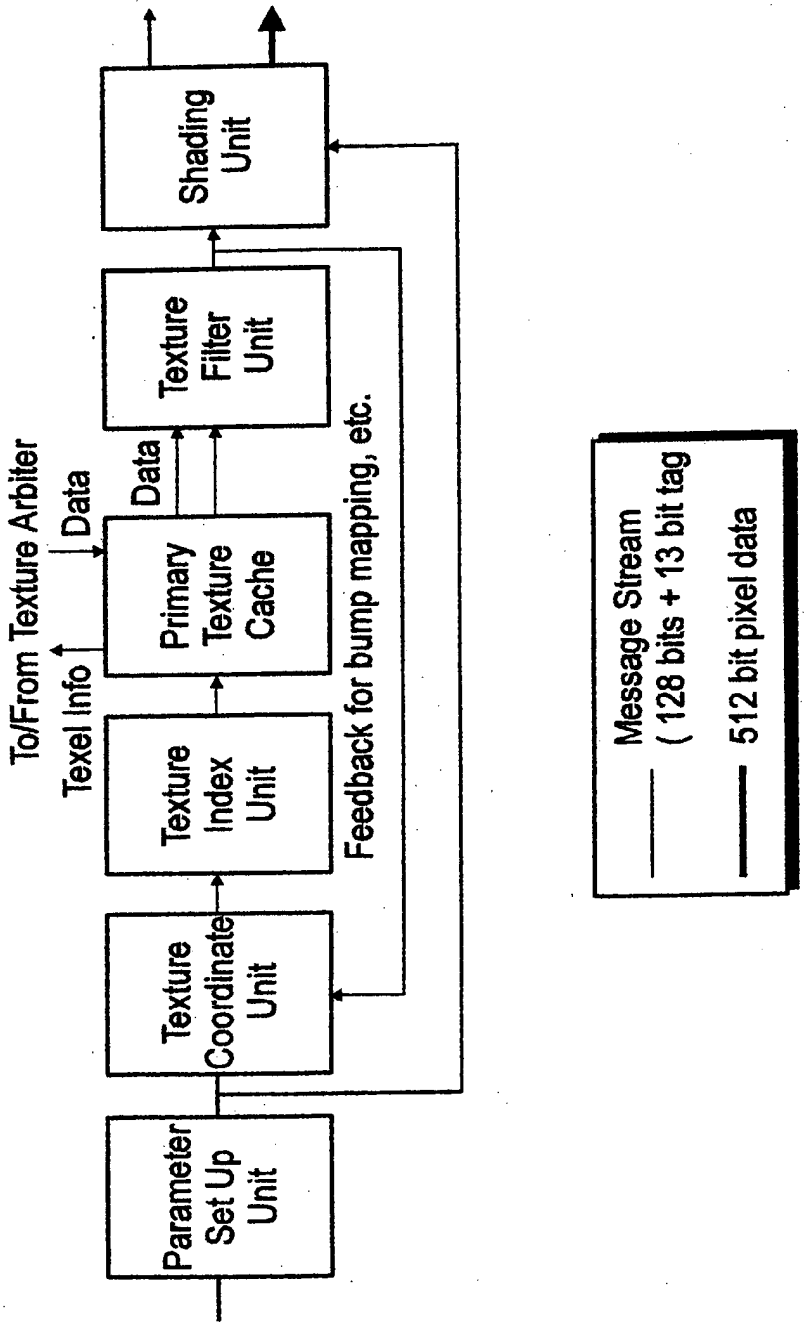
Parameter Set Up Unit
Texture Coordinate Unit
Texture Index Unit
Primary Texture Cache
Texture Filter Unit
Shading Unit
To/From Texture Arbiter
Texel Info
Data
Data
Feedback for bump mapping, etc.
Message Stream
( 128 bits + 13 bit tag
512 bit pixel data

FIG. 1D

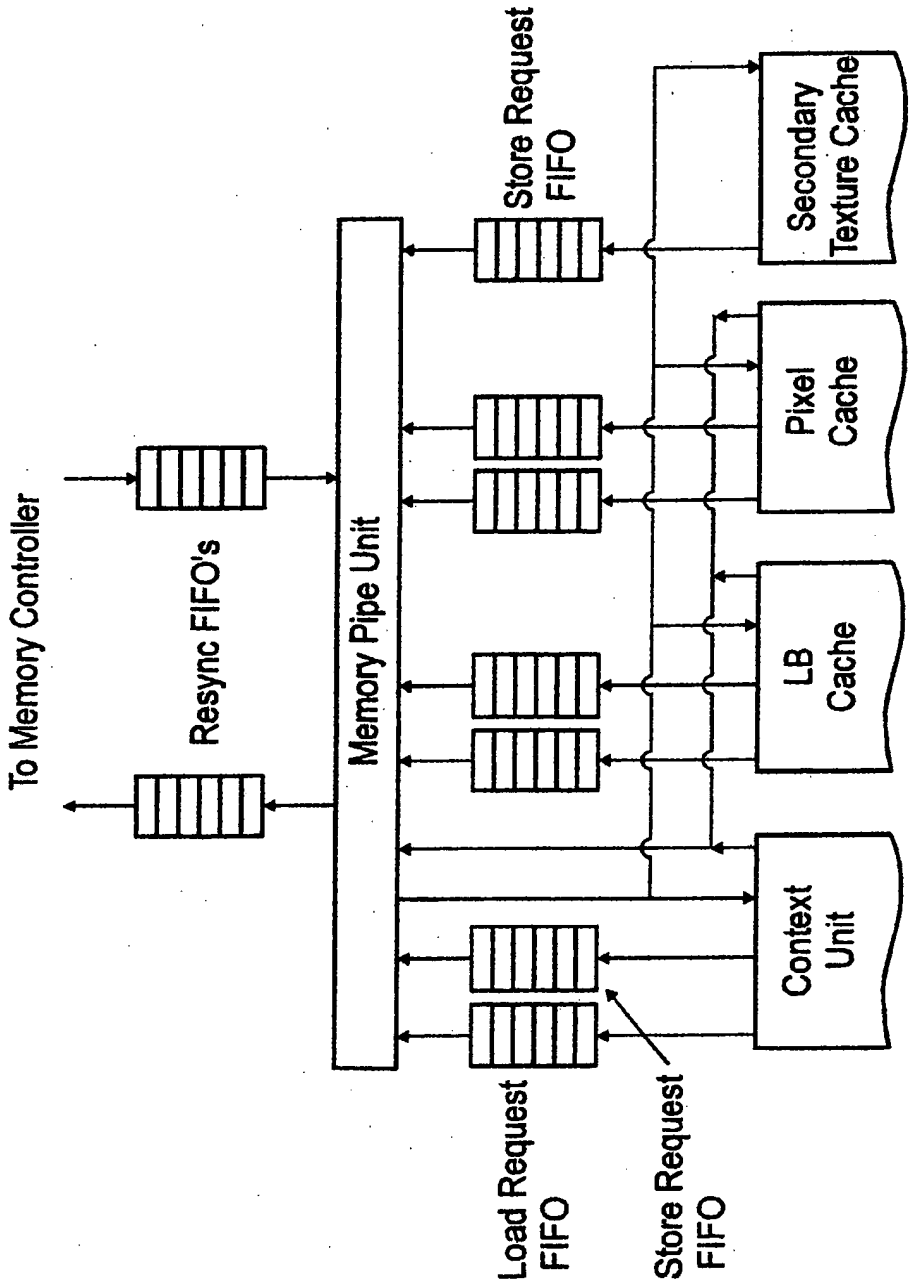
To Memory Controller
Resync FIFO's
Memory Pipe Unit
Store Request FIFO
Secondary Texture Cache
Pixel Cache
LB Cache
Context Unit
Load Request FIFO
Store Request FIFO

FIG. 1E

APPENDIX E – Related Appeals Appendix

None